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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,040	11/18/2003	Tony K. Ngai	X-1363 US	7436

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,040	NGAI ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11182003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-42 have been examined.

Claim Objections

2. Claims 5, 19, 28 and 37 are objected to because in the limitation "setting the first error flag comprises setting an error flag associated with a defective plurality of columns of the RAM cells" the setting of the first error flag implies a *single* flag associated with a *single* column of RAM cells, not a plurality. In claims 1, 15, 25, and 34 the error flag is associated with a first (single) defective column of the RAM cells and the first error flag is in a first (single) volatile memory circuit. This limitation should read "setting the first error flag comprises setting a plurality of error flags associated with each of a defective plurality of columns of the RAM cells".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 25-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 25:

a.) Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: initiating a normal user operation. The Examiner fails to understand how can one resume a normal user operation (line 8) when the normal user operation was never started or initiated.

b.) This claim recite the limitations "normal user operation" in line 8 and "user operation" in line 14. There is insufficient antecedent basis for these limitations in these claims.

c.) The limitations "normal user operation" in line 8 and "user operation" in line 14 are not defined and renders the claim indefinite. The Examiner does not understand what a normal user operation entails.

Because of the ambiguities of claim 25 the "resuming normal user operation" and "resuming user operation" limitations will not be further examined on the merits.

Claim 34:

a.) Claim 34 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: means for initiating a normal user operation. The Examiner fails to understand how can one resume a normal user operation (line 7) when the normal user operation was never started or initiated.

b.) This claim recite the limitations "normal user operation" in line 7 and "user operation" in line 15. There is insufficient antecedent basis for these limitations in these claim.

c.) The limitations "normal user operation" in line 7 and "user operation" in line 15 are not defined and renders the claim indefinite. The Examiner does not understand what a normal user operation entails.

Because of the ambiguities of claim 34 the "resuming normal user operation" and "resuming user operation" limitations will not be further examined on the merits.

Claims 26 and 35:

a.) These claims recite the limitation "user operation". There is insufficient antecedent basis for this limitation in these claims.

b.) The limitation "user operation" is not defined and renders these claims indefinite. The Examiner does not understand what a user operation entails.

Because of the ambiguities of claims 26 and 35 the "resuming user operation" limitation will not be further examined on the merits.

Claims 26-33 and 35-42:

These claims are also rejected because they depend on the rejected base claims 25 and 34 and have the same problems of missing essential steps/parts, insufficient antecedent basis, and indefiniteness.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-7, 9, 10, 11, 13-15, 17-21, 23-25, 27-30, 32-34, 36-39, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cliff et al. (US005498975), hereinafter Cliff, in view of Rao et al. (US006055205), hereinafter Rao.

Claims 1 and 15:

Cliff teaches configuring a programmable logic device (PLD) which comprises a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells (SRAM-based PLD, Fig. 1 and 5, col. 2, 41-61) and a first redundant column of the RAM cells (Fig. 5, 430(1)). Cliff also teaches initiating a configuration sequence for the PLD. (Col. 2, 41-61, col. 7, ll. 24-65). Cliff further teaches when an error associated with the first array is reported (a column is found defective, col. 7, ll. 24-65), setting a first error flag in a first volatile memory circuit (programmable data bit in decoders 410(A)-(I), which can be implemented in RAM, col. 7, ll. 24-65) associated with a first defective column of the RAM cells in the first array. Cliff discloses loading first PLD configuration data into the first RAM circuit, wherein when the first error flag is set the first PLD configuration data bypasses the first defective column of the RAM cells and a first portion of the first PLD configuration data is loaded into the first redundant column of the RAM cells. (Col. 7, ll. 24-65).

Cliff does not explicitly teach "initiating a built in self test (BIST) procedure on the first array". However, Cliff does teach when a column of logic blocks, such as column 430(3), is found to be defective, redundant column 430(1) is switched into the matrix. Rao teaches in an analogous art that a conventional mechanism uses a volatile built in self-repair structure (BISR) structure in conjunction with the BIST structure. In this case, each time the chip is powered up, the BIST structure electrically tests the memory array, and provides the defective column addresses to the BISR structure. In response, the BISR structure is configured to electrically re-route the address signals provided to the memory array. More specifically, the BISR structure is configured such that when a defective column address is provided to the BISR structure, the BISR structure translates this defective column address to a functional redundant column address. The BISR structure is configured by programming volatile memory elements present in the BISR structure. (Col. 18, ll. 46-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cliff's procedure of finding a defective column to testing with Rao's BIST structure and method. The artisan would be motivated to do so because it would enable Cliff to test the SRAM-based PLD internally.

Claims 25 and 34:

Cliff teaches configuring a programmable logic device (PLD) which comprises a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells (SRAM-based PLD, Fig. 1 and 5, col. 2, 41-61) and a first redundant column of the RAM cells (Fig. 5, 430(1)). Cliff also teaches when an error associated with the first array is reported (a column is found defective, col. 7, ll. 24-65),

setting a first error flag in a first volatile memory circuit (programmable data bit in decoders 410(A)-(I), which can be implemented in RAM, col. 7, ll. 24-65) associated with a first defective column of the RAM cells in the first array. Cliff further teaches when an error associated with the first array is reported by the BIST procedure, while using the first error flag to bypass the first defective column and to shunt read and write data from and to the first redundant column instead of the first defective column. (Col. 7, ll. 24-65).

Cliff does not explicitly teach "initiating a built in self test (BIST) procedure on the first array". However, Cliff does teach when a column of logic blocks, such as column 430(3), is found to be defective, redundant column 430(1) is switched into the matrix. Rao teaches in an analogous art that a conventional mechanism uses a volatile built in self-repair structure (BISR) structure in conjunction with the BIST structure. In this case, each time the chip is powered up, the BIST structure electrically tests the memory array, and provides the defective column addresses to the BISR structure. In response, the BISR structure is configured to electrically re-route the address signals provided to the memory array. More specifically, the BISR structure is configured such that when a defective column address is provided to the BISR structure, the BISR structure translates this defective column address to a functional redundant column address. The BISR structure is configured by programming volatile memory elements present in the BISR structure. (Col. 18, ll. 46-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cliff's procedure of finding a

defective column to testing with Rao's BIST structure and method. The artisan would be motivated to do so because it would enable Cliff to test the SRAM-based PLD internally.

Claim 25:

Cliff teaches a programmable logic device (PLD), which comprises a first read/write data access port, a first random access memory (RAM) circuit comprising a first array of rows and columns of RAM cells and a first redundant column of the RAM cells. (SRAM-based PLD, Fig. 1 and 5, col. 2, 41-61). Cliff also teaches a first routing circuit coupled between the first data access port and the first RAM circuit, the first routing circuit comprising a plurality of programmable interconnections between the first data access port and selected columns of the first RAM circuit, and also includes a plurality of volatile memory circuits coupled to program the programmable routing interconnections. (Fig. 5, programmable data bit in decoders 410(A)-(I), which can be implemented in RAM, col. 7, ll. 24-65). Even though Cliff does show a configuration controller it is inherently there because it is well known in the art that all PLDs must have a configuration controller present to perform this procedure. (See Veenstra et al. (US-6605960, Nishihara (US-6304101) and Jenkins (US-6020757), for example).

Cliff does not explicitly teach "a built in self test (BIST) control circuit coupled to the volatile memory circuits of the first routing circuit and further coupled to the first RAM circuit". However, Cliff does teach when a column of logic blocks, such as column 430(3), is found to be defective, redundant column 430(1) is switched into the matrix. Rao teaches in an analogous art that a conventional mechanism uses a volatile built in self-repair structure (BISR) structure in conjunction with the BIST structure. In this case,

each time the chip is powered up, the BIST structure electrically tests the memory array, and provides the defective column addresses to the BISR structure. In response, the BISR structure is configured to electrically re-route the address signals provided to the memory array. More specifically, the BISR structure is configured such that when a defective column address is provided to the BISR structure, the BISR structure translates this defective column address to a functional redundant column address. The BISR structure is configured by programming volatile memory elements present in the BISR structure. (Col. 18, ll. 46-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cliff's procedure of finding a defective column to testing with Rao's BIST structure. The artisan would be motivated to do so because it would enable Cliff to test the SRAM-based PLD internally. It also would have been obvious to one of ordinary skill in the art at the time the invention was made to couple to the BIST control circuit (Rao's BIST structure) to Cliff's configuration control circuit (inherently there). The artisan would be motivated to do so because it would enable Rao's BIST structure and Cliff's configuration control circuit to perform hand-shaking procedures to better control the testing and configuring.

Claims 3 and 17:

Cliff teaches initiating a configuration sequence for the PLD comprising powering up the PLD. (Col. 1, ll. 20-23, col. 2, ll. 56-58).

Claims 4, 18, 27 and 36:

Cliff teaches the PLD is a field programmable gate array (FPGA). (Col. 1, ll. 15-17).

Claims 5, 19, 28 and 37:

Cliff teaches "the first RAM circuit includes a plurality of redundant columns of the RAM cells, and setting the first error flag comprises setting an error flag associated with a defective plurality of columns of the RAM cells". (Col. 8, ll. 3-9).

Claims 6, 20, 29 and 38:

Cliff teaches "the plurality of redundant columns of the RAM cells are adjacent to one another within the first RAM circuit". (Col. 8, ll. 3-11, Fig. 5).

Claims 7, 21, 30 and 39:

Cliff teaches "the plurality of redundant columns of the RAM cells are organized into groups that are equally spaced from one another within the first RAM circuit". (Col. 8, ll. 3-11, Fig. 5).

Claims 9, 13, 23, 32 and 41:

Cliff teaches the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the array. (Fig. 5, Col. 7, ll. 24-65)

Claims 10, 14, 24, 33 and 42:

Cliff teaches the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the array. (Fig. 5, Col. 7, ll. 24-65, col. 8, ll. 17-19)

5. Claims 2, 12, 16, 26 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cliff et al. (US005498975), hereinafter Cliff, in view of Rao et al. (US006055205), hereinafter Rao, in further view of Venkatraman et al. (US 20020120826), hereinafter Venkatraman.

Claims 2, 16, 26 and 35:

Cliff in view of Rao does not explicitly teach "initiating the BIST procedure on the second array concurrently with initiating the BIST procedure on the first array". However, Cliff in view of Rao substantially teaches the setting, loading and initiating the BIST procedure steps for the first array. Venkatraman teaches in an analogous art the concurrent BIST testing of multiple memory arrays of a reconfigurable memory (PLD). It would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate Cliff's memory array as in Venkatraman as to effectuate concurrent BIST testing and reconfiguring of multiple memory arrays with redundant columns. The artisan would be motivated to do so because since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (7th Cir. 1977).

Claim 12:

Cliff in view of Rao does not explicitly teach "the BIST control circuit is coupled to the volatile memory circuits of the second routing circuit and to the second RAM circuit". However, Cliff in view of Rao substantially teaches a data access port, RAM circuit, routing circuit and a configuration control circuit for the first array as per the rejection of claim 11. Venkatraman teaches in an analogous art the concurrent BIST testing of multiple memory arrays of a reconfigurable memory (PLD). It would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate Cliff's memory array as in Venkatraman as to effectuate concurrent BIST testing and reconfiguring of multiple memory arrays with redundant columns with the connections

as per claim 12. The artisan would be motivated to do so because since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (7th Cir. 1977).

6. Claims 8, 22, 31 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cliff et al. (US-5498975), hereinafter Cliff, in view of Rao et al. (US-6055205), hereinafter Rao, in further view of Applicant's Admitted Prior Art, hereinafter AAPA.

Claims 8, 22, 31 and 40:

Cliff in view of Rao does not explicitly teach "the BIST procedure comprises writing and reading a checkerboard pattern and a reverse checkerboard pattern". However, Cliff in view of Rao does teach a conventional BIST structure for testing the memory array. (Col. 18, l. 49). AAPA teaches in an analogous art that writing and reading a checkerboard pattern and a reverse checkerboard pattern is well known in the art. (pg. 6, ¶ 25). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Rao's BIST structure would run a checkerboard pattern and a reverse checkerboard pattern. The artisan would be motivated to do so because reading a checkerboard pattern and a reverse checkerboard pattern is well known in the art and common in the state of the art BIST controllers.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cliff et al. (US005485102)

Cliff substantially teaches a majority of the limitations of claims 1-42, in particular claims 6, 20, 29 and 38 where redundant columns of the RAM cells are adjacent to one another and claims 7, 21, 30 and 39 where redundant columns of the RAM cells are organized into groups that are equally spaced from one another. (Col. 7, ll. 41-43).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr. 4/26/06
Examiner
Art Unit 2138

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